Remarks

Applicant thanks the Examiner for the careful examination of this application and the clear explanation of the rejections.

The amended title is clearly indicative of the invention to which the claims are directed.

The amended claims "particularly point out and distinctly claim the subject matter the applicant regards as his invention."

Independent claim 12 defines a process of testing an integrated circuit.

The process applies stimulus test signals to input pads of the integrated circuit.

The process conveys the applied stimulus test signals to core circuits in the integrated circuit.

The process produces core test response output signals from the core circuits in response to the stimulus test signals.

The process applies expected response test signals to output pads of the integrated circuit.

The process compares on the integrated circuit the core test response output signals to the expected response test signals received on the output pads to produce a pass/fail signal.

In contrast, US 6,215,324 to Yoshida discloses, in regard to Figure 3:

conventional general burn-in test equipment. A "high (H)" or "low (L)" value stored in a pattern memory 61 is transferred to an input terminal (input pin) of the DUT 21 through a driver 51, information appeared (sic) at an output terminal (output pin) of the DUT 21 is compared with an expected value by a comparator 53. An "H" or "L" expected value is stored in an expectation memory 64 in advance. The behavior or the result of the compared output terminal is stored in a result memory 65. Column 3, lines 30-38.

In regard to Figure 8, the patent to Yoshida discloses:

In FIG. 8, a predetermined input signal is applied from a pattern memory 61 to the input terminal of the DUT 21 through the driver 51, and a predetermined expected value is applied from the expectation memory 64 to the output terminal of the DUT 21 through a driver 55. When the internal circuit of the DUT 21 normally operates, an output signal from the DUT 21 and a signal given from the expectation memory 64 through the driver 55 are in an equilibrium state at the output terminal of the DUT 21. For this reason, a current does not flow. Column 10, lines 3 and following.

Thus the patent to Yoshida discloses applying to the output pad of an IC an expected response signal. If the expected response signal is the same as the signal output from the DUT, the two signals are in equilibrium and the voltage/current detectors 11 and 15 indicate proper function of the IC.

In amended claim 12, the process: applies stimulus test signals to input pads of the integrated circuit; applies expected response test signals to output pads of the integrated circuit; and compares on the integrated circuit the core test response output signals to the expected response test signals received on the output pads to produce a pass/fail signal.

Claim 12 stands allowable.

The application is in allowable form and the claims distinguish over the cited references. Applicant

respectfully requests reconsideration or further examination of this application.

Respectfully Submitted,

/Lawrence J. Bassuk/

Lawrence J. Bassuk
Reg. No. 29,043
Attorney for Applicant

Texas Instruments Incorporated
P. O. Box 655474, MS 3999
Dallas, Texas 75265
972-917-5458